

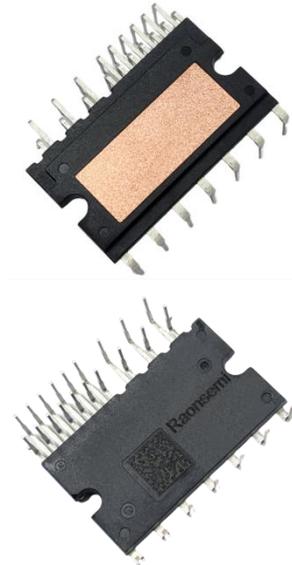
# RSN56007CT

## Green Power Module (GPM) 650V 3-Phase Full SiC Inverter



### Features

- 650V / 60mΩ SiC MOSFETs
- Built-In Bootstrap Diodes
- Very Low Thermal Resistance with DBC Substrate
- Separate Open-Sources from Low-Side MOSFETs
- Under-Voltage Lock-Out for high side and low side
- Short-Circuit Protection
- Over Temperature Protection
- LVIC Temperature Output
- 3.3 V and 5V Input Logic Compatible : Active High
- Fault Signaling : LVIC UVLO and Short-circuit Protection
- Isolation Rating of 2000 Vrms/1 min
- UL 1557 Certified (File E540859)



### Typical Applications

- Air-conditioner, Washing machine etc.
- Motor Control – Industrial Motor (AC 200 V Class)

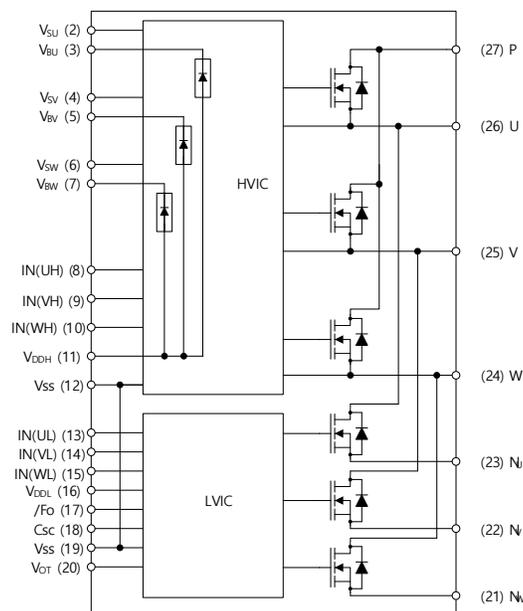


Figure 1. Internal Circuit

## PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
2	V <sub>SU</sub>	High-Side Bias Voltage Ground for U Phase MOSFET Driving
3	V <sub>BU</sub>	High-Side Bias Voltage for U Phase MOSFET Driving
4	V <sub>SV</sub>	High-Side Bias Voltage Ground for V Phase MOSFET Driving
5	V <sub>BV</sub>	High-Side Bias Voltage for V Phase MOSFET Driving
6	V <sub>SW</sub>	High-Side Bias Voltage Ground for W Phase MOSFET Driving
7	V <sub>BW</sub>	High-Side Bias Voltage for W Phase MOSFET Driving
8	IN(UH)	Signal Input for High-Side U Phase
9	IN(VH)	Signal Input for High-Side V Phase
10	IN(WH)	Signal Input for High-Side W Phase
11	V <sub>DDH</sub>	High-Side Bias Voltage for IC
12	V <sub>SS</sub>	High-Side Common Supply Ground, connected to LVIC
13	IN(UL)	Signal Input for Low-Side U Phase
14	IN(VL)	Signal Input for Low-Side V Phase
15	IN(WL)	Signal Input for Low-Side W Phase
16	V <sub>DDL</sub>	Low-Side Bias Voltage for IC and MOSFETs Driving
17	/FO	Fault Output
18	Csc	Input for Current Protection
19	V <sub>SS</sub>	Low-Side Common Supply Ground, connected to LVIC
20	V <sub>OT</sub>	Voltage Output for LVIC Temperature
21	N <sub>W</sub>	Negative DC-Link Input for W Phase
22	N <sub>V</sub>	Negative DC-Link Input for V Phase
23	N <sub>U</sub>	Negative DC-Link Input for U Phase
24	W	Output for W Phase
25	V	Output for V Phase
26	U	Output for U Phase
27	P	Positive DC-Link Input

**ABSOLUTE MAXIMUM RATINGS** ( $T_j = 25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
<b>INVERTER PART</b>				
$V_{PN}$	Supply Voltage	Applied between P- $N_U, N_V, N_W$	450	V
$V_{PN(surge)}$	Supply Voltage (Surge)	Applied between P- $N_U, N_V, N_W$	550	V
$V_{DSS}$	Drain-source Voltage		650	V
$I_D$	Each MOSFET Drain Current	$T_c=25^{\circ}\text{C}, T_j \leq 150^{\circ}\text{C}$	(30)	A
$I_{DP}$	Each MOSFET Drain Current (Peak)	$T_c=25^{\circ}\text{C}, T_j \leq 150^{\circ}\text{C}$ , Under 1ms Pulse Width (Note 1)	(60)	A
$P_D$	Power Dissipation per MOSFET	$T_c=25^{\circ}\text{C}$ per One Chip (Note 1)	(71)	W
$T_j$	Operating Junction Temperature		-40~150	$^{\circ}\text{C}$

**CONTROL PART**

$V_{DD}$	Control Supply Voltage	Applied between $V_{DDH}, V_{DDL}-V_{SS}$	(22)	V
$V_{BS}$	High-Side Control Bias Voltage	Applied between $V_{BU}-V_{SU}, V_{BV}-V_{SV}, V_{BW}-V_{SW}$	(22)	V
$V_{IN}$	Input Signal Voltage	Applied between IN(UH), IN(VH), IN(WH), IN(UL), IN(VL), IN(WL) - $V_{SS}$	$-0.5-V_{DD}+0.5$	V
$V_{FO}$	Fault Output Supply Voltage	Applied between $F_O-V_{SS}$	$-0.5-V_{DD}+0.5$	V
$I_{FO}$	Fault Output Current	Sink Current at $F_O$ pin	5	mA
$V_{SC}$	Current Sensing Input Voltage	Applied between $C_{SC}-V_{SS}$	$-0.5-V_{DD}+0.5$	V
$T_j$	Operating Junction Temperature		-40~150	$^{\circ}\text{C}$

**BOOSTSTRAP DIODE PART**

$V_{RRM}$	Maximum Repetitive Reverse Voltage		650	V
$T_j$	Operating Junction Temperature		-40~150	$^{\circ}\text{C}$

**TOTAL SYSTEM**

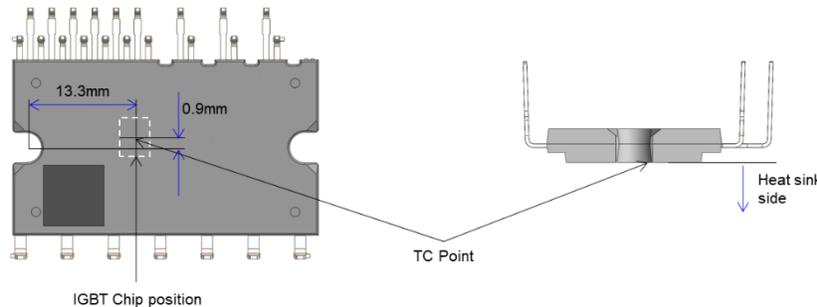
$V_{PN(PROT)}$	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{DD}=V_{BS}=17\sim 19\text{V}, T_j=150^{\circ}\text{C}$ , Non-Repetitive, $< 2 \mu\text{s}$	400	V
$T_c$	Module Case Operation Temperature	See Figure 2	-40~125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature		-40~125	$^{\circ}\text{C}$
$V_{iso}$	Isolation Voltage	60 Hz, Sinusoidal, AC 1 Minute, Connection Pins to Heat Sink Plate	2000	Vrms

Note 1: These values had been made an acquisition by the calculation considered to design factor.

**THERMAL RESISTANCE**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance (Note 2)	Inverter MOSFET Part (per 1/6 module)	-	-	(1.75)	$^{\circ}\text{C/W}$

Note 2: For the measurement point of case temperature ( $T_c$ ), please refer to Figure 2.



**Figure 2.  $T_c$  Measurement Point**

**ELECTRICAL CHARACTERISTICS** ( $T_j = 25^\circ\text{C}$  unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
$R_{DS(ON)}$	Drain-source On Resistance	$V_{DD}=V_{BS}=18\text{V}$ $V_{IN}=5\text{V}$ $I_C=30\text{A}$ $T_j=25^\circ\text{C}$	-	(57)	(78)	$\text{m}\Omega$		
$V_{SD}$	Diode Forward Voltage	$V_{IN}=0\text{V}$ $I_C=-30\text{A}$ $T_j=25^\circ\text{C}$	-	(4.8)	-	V		
HS	Switching Times	$V_{PN}=300\text{V}$ , $V_{DD}=18\text{V}$ , $I_C=30\text{A}$ $T_j=25^\circ\text{C}$ $V_{IN}=0\text{V}\leftrightarrow 5\text{V}$ , Inductive Load, See Figure 3 (Note 3)	$t_{on}$	-	(1.2)	-	$\mu\text{s}$	
			$t_{c(on)}$	-	(0.1)	-	$\mu\text{s}$	
			$t_{off}$	-	(1.2)	-	$\mu\text{s}$	
			$t_{c(off)}$	-	(0.05)	-	$\mu\text{s}$	
			$t_{rr}$	-	(50)	-	ns	
LS	Switching Times		$V_{PN}=300\text{V}$ , $V_{DD}=18\text{V}$ , $I_C=30\text{A}$ $T_j=25^\circ\text{C}$ $V_{IN}=0\text{V}\leftrightarrow 5\text{V}$ , Inductive Load, See Figure 3 (Note 3)	$t_{on}$	-	(1.2)	-	$\mu\text{s}$
				$t_{c(on)}$	-	(0.1)	-	$\mu\text{s}$
				$t_{off}$	-	(1.2)	-	$\mu\text{s}$
				$t_{c(off)}$	-	(0.05)	-	$\mu\text{s}$
				$t_{rr}$	-	(50)	-	ns
$I_{DSS}$	Drain-source Leakage Current	$V_{DS} = V_{DSS}$		-	-	1	mA	

Note 3:  $t_{on}$  and  $t_{off}$  include the propagation delay of the internal drive IC.  $t_{c(on)}$  and  $t_{c(off)}$  are the switching times of MOSFET under the given gate-driving condition internally. For the detailed information, please see Figure 3.

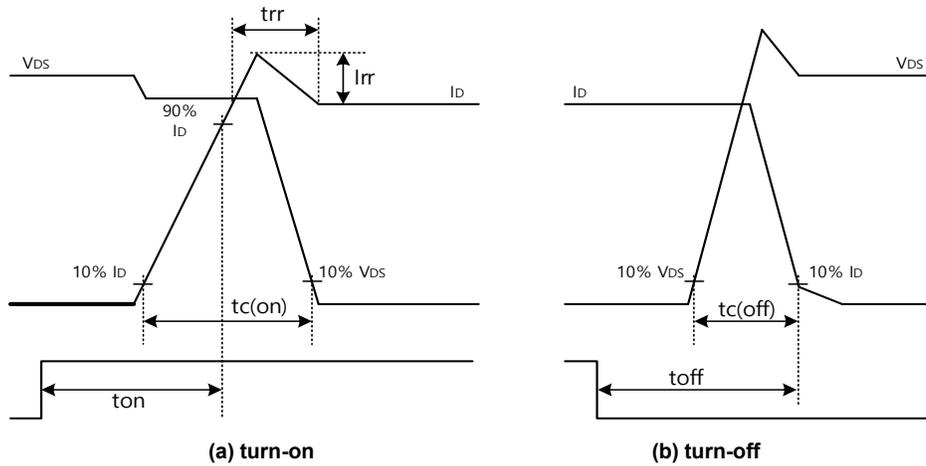


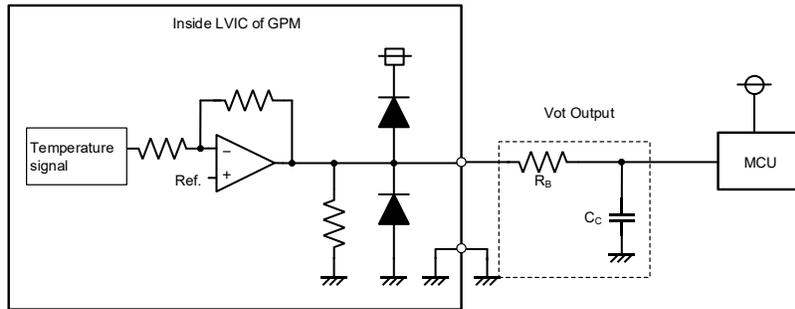
Figure 3. Switching Time Definition

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{QDDH}$	Quiescent $V_{DD}$ Supply Current	$V_{DDH}=18\text{V}$ , $V_{IN(UH,VH,WH)}=0\text{V}$	-	-	0.1	mA
$I_{QDDL}$		$V_{DDL}=18\text{V}$ , $V_{IN(UL,VL,WL)}=0\text{V}$	-	-	2.0	mA
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{DDH}=V_{DDL}=V_{BS}=18\text{V}$ , $V_{IN(UH,VH,WH)}=0\text{V}$	-	-	0.1	mA
$V_{FOH}$	Fault Output Voltage	$V_{DDL}=18\text{V}$ , $V_{sc}=0\text{V}$ , $V_{FO}$ Circuit: 10k $\Omega$ to 5V Pull-up	4.90	-	-	V
$V_{FOL}$		$V_{DDL}=18\text{V}$ , $V_{sc}=1\text{V}$ , $I_{FO}=1\text{mA}$	-	-	0.95	V
$V_{SC(ref)}$	Short Circuit Trip Level (Note 4)	$V_{DDL}=18\text{V}$	0.455	0.48	0.505	V

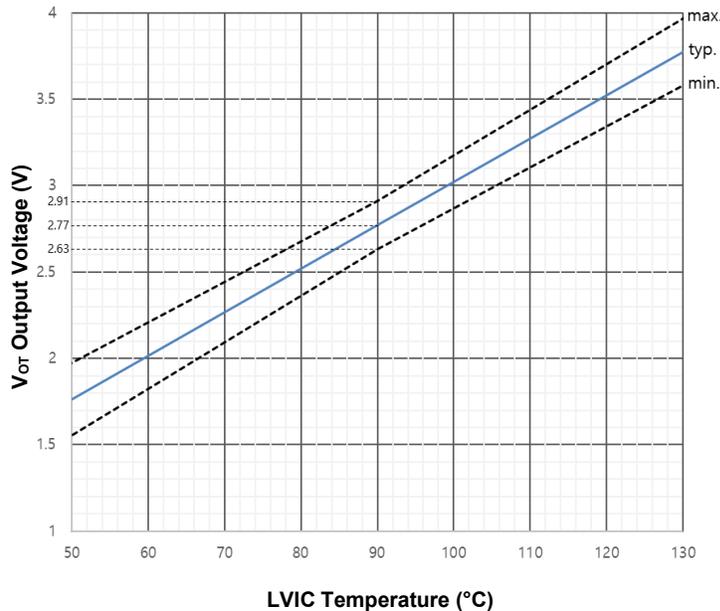
**ELECTRICAL CHARACTERISTICS** (T<sub>j</sub> = 25°C unless otherwise specified.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>CONTROL PART</b>							
U <sub>VDDD</sub>	Supply Circuit Under-Voltage Protection	Detection Level	10.3	-	12.5	V	
U <sub>VDDR</sub>		Reset Level	10.8	-	13.0	V	
U <sub>VBSD</sub>		Detection Level	10.0	-	12.0	V	
U <sub>VBSR</sub>		Reset Level	10.5	-	12.5	V	
I <sub>IN</sub>	Input Current (Note 6)	V <sub>IN</sub> = 5V	0.7	1.0	1.5	mA	
V <sub>IN(ON)</sub>	ON Threshold Voltage	Applied between V <sub>IN(UH,VH,WH)</sub> -V <sub>SS</sub> , V <sub>IN(UL,VL,WL)</sub> -V <sub>SS</sub>	-	-	2.6	V	
V <sub>IN(OFF)</sub>	OFF Threshold Voltage		0.8	-	-	V	
OT <sub>trip</sub>	Over temperature protection	V <sub>DDL</sub> =18V Detect LVIC temperature	Trip level	130	140	150	°C
OT <sub>hys</sub>		Hysteresis of trip-reset		10		°C	
V <sub>OT</sub>	Voltage Output for LVIC Temperature Sensing Unit	V <sub>DDL</sub> =18V, T <sub>LVIC</sub> =25°C See Figure 4 and 5 (Note 5)	0.88	1.13	1.39	V	
t <sub>FOD</sub>	Fault-Out Pulse Width		20	-	-	us	

- Note 4: Short-circuit protection functions only at the low-sides because the sense current is divided from main current at low-side MOSFETs. Inserting the shunt resistor for monitoring the phase current at NU, NV, NW terminal, the trip level of the short-circuit current is changed.
- Note 5: T<sub>LVIC</sub> is LVIC temperature and V<sub>OT</sub> is only for sensing the temperature of LVIC and cannot shut down MOSFETs automatically. The relationship between V<sub>OT</sub> voltage output and LVIC temperature is described in Figure 5. It is recommended to add a ceramic capacitor of 10 nF or more between V<sub>OT</sub> and V<sub>SS</sub> to make the V<sub>OT</sub> more stable. Refer to the application note for this product about usage of V<sub>OT</sub>.
- Note 6: RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section integrates 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at the input terminal.



**Figure 4. Internal Block Diagram and Interface Circuit of V<sub>OT</sub>**



**Figure 5. Temperature Profile of V<sub>OT</sub>**

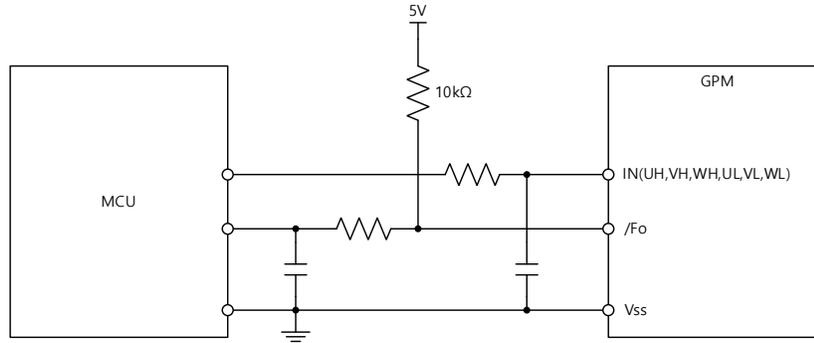


Figure 6. Recommended MCU I/O Interface Circuit

**ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C unless otherwise specified.) (continued)**  
**BOOTSTRAP DIODE/RESISTOR PART**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>F</sub>	Forward Voltage	I <sub>F</sub> =0.01A, T <sub>j</sub> =25°C	See Figure 7	-	2.5	-	V

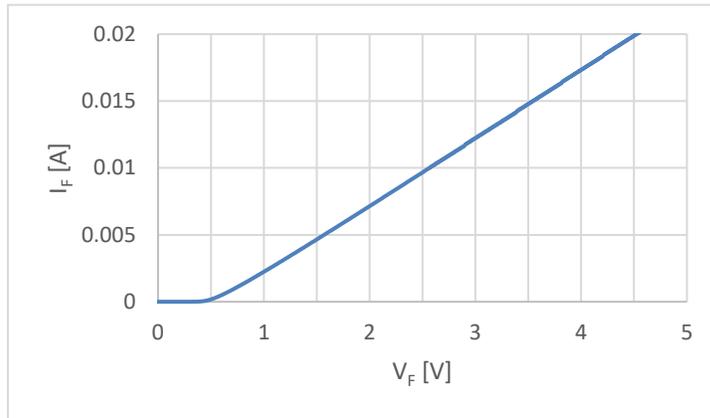


Figure 7. Characteristics of Bootstrap Diode

**RECOMMENDED OPERATING RANGES**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>PN</sub>	Supply Voltage	Applied between P-N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub>	-	300	400	V
V <sub>DD</sub>	Control Supply Voltage	Applied between V <sub>DDH</sub> -V <sub>SS</sub> , V <sub>DDL</sub> -V <sub>SS</sub>	13.5	15.0	16.5	V
V <sub>BS</sub>	High-Side Control Bias Voltage	Applied between V <sub>BU</sub> -V <sub>SU</sub> , V <sub>BV</sub> -V <sub>SV</sub> , V <sub>BW</sub> -V <sub>SW</sub>	13.0	15.0	18.5	V
dV <sub>DD</sub> /dt, dV <sub>BS</sub> /dt	Control Supply Variation		-1	-	+1	V/μs
t <sub>dead</sub>	Blanking Time for Preventing Arm - Short	For Each Input Signal	1.0	-	-	μs
f <sub>PWM</sub>	PWM Input Signal	-40°C ≤ T <sub>C</sub> ≤ 125°C, -40°C ≤ T <sub>j</sub> ≤ 150°C	-	-	20	kHz
PWIN(ON)	Minimum Input Pulse Width	(Note 7)	0.7	-	-	μs
PWIN(OFF)			0.7	-	-	
T <sub>j</sub>	Junction Temperature		-40	-	+150	°C

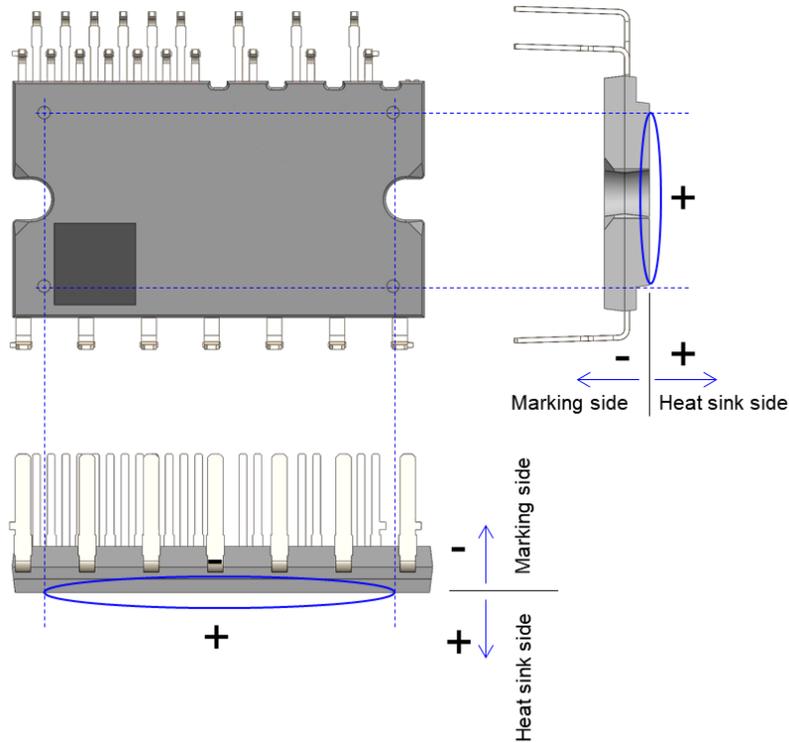
Note 7: This product might not make output response if input pulse width is less than the recommended value.

**PACKAGE MARKING AND ORDERING INFORMATION**

Device	Device Marking	Package	Shipping
RSN56007CT	RSN56007CT	GPM26-AB	704 ea/box

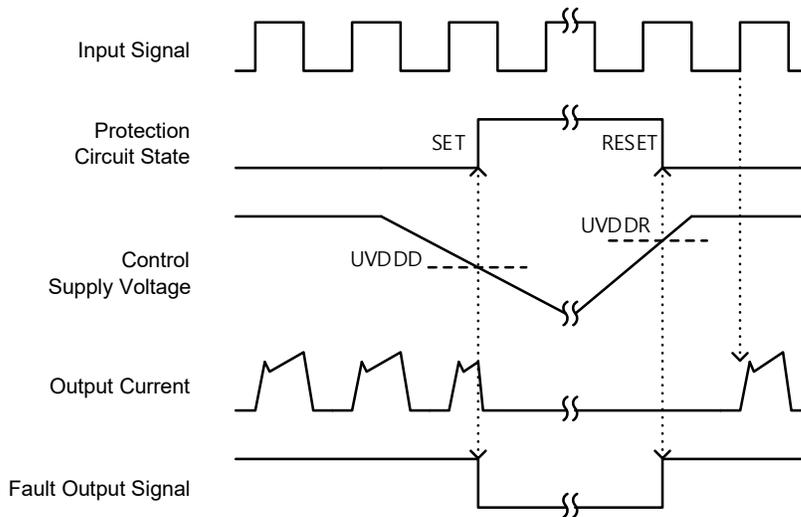
**MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Conditions	Min	Typ	Max	Unit
Device Flatness	See Figure 8	-50	-	100	μm
Mounting Torque	Mounting Screw: M3	0.59	0.69	0.78	N·m
Terminal Pulling Strength	Control terminal : Load 5N Power terminal : Load 10N	10	-	-	s
Terminal Bending Strength	Control terminal : Load 5N Power terminal : Load 10N 90 degree Bend	2	-	-	times
Weight		-	5.5	-	g



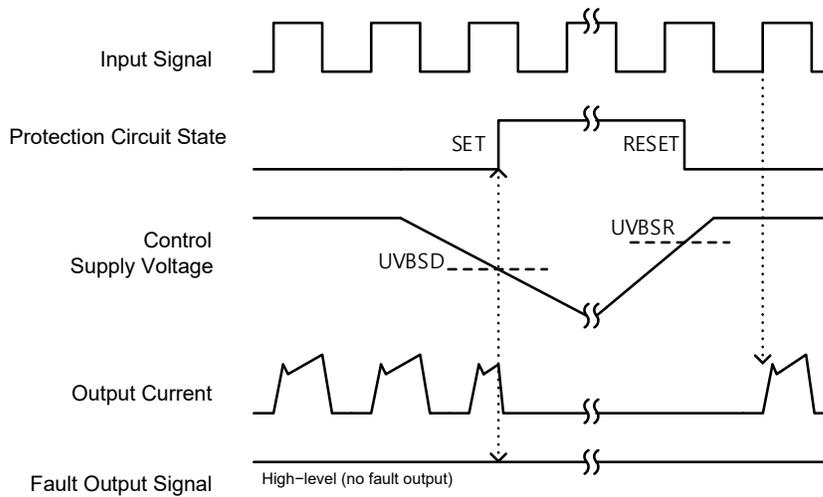
**Figure 8. Flatness Measurement Position**

TIME CHARTS OF GPMs PROTECTIVE FUNCTION



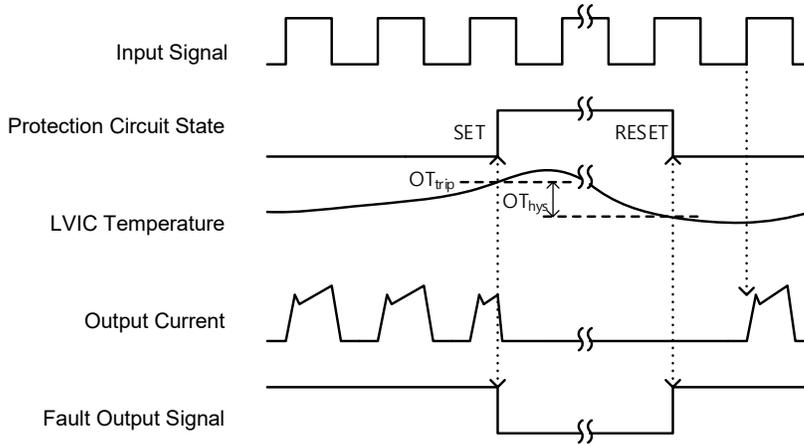
- 1: Normal operation: MOSFET ON and carrying current.
- 2: Under-voltage detection (UVDDD).
- 3: MOSFET OFF in spite of control input condition.
- 4: Fault output operation starts with a fixed pulse width (min. 20us).
- 5: Under-voltage reset (UVDDR).
- 6: Normal operation: MOSFET ON and carrying current by triggering next signal from LOW to HIGH.

Figure 9. Under-voltage Protection (Low-side)



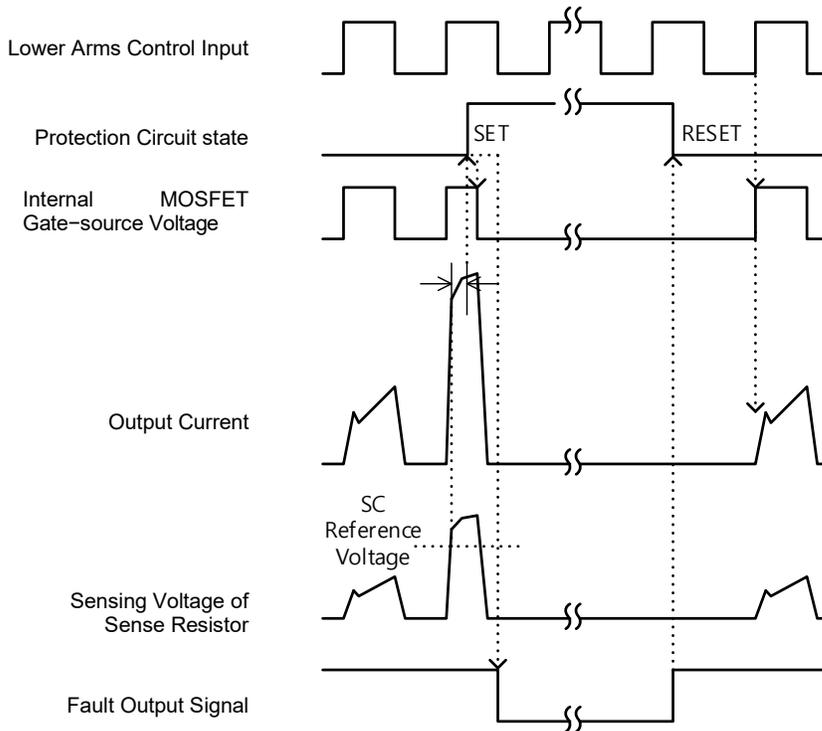
- 1: Normal operation: MOSFET ON and carrying current.
- 2: Under-voltage detection (UVBSD).
- 3: MOSFET OFF in spite of control input condition, but there is no fault output signal.
- 4: Under-voltage reset (UVBSR).
- 5: Normal operation: MOSFET ON and carrying current by triggering next signal from LOW to HIGH.

Figure 10. Under-voltage Protection (High-side)



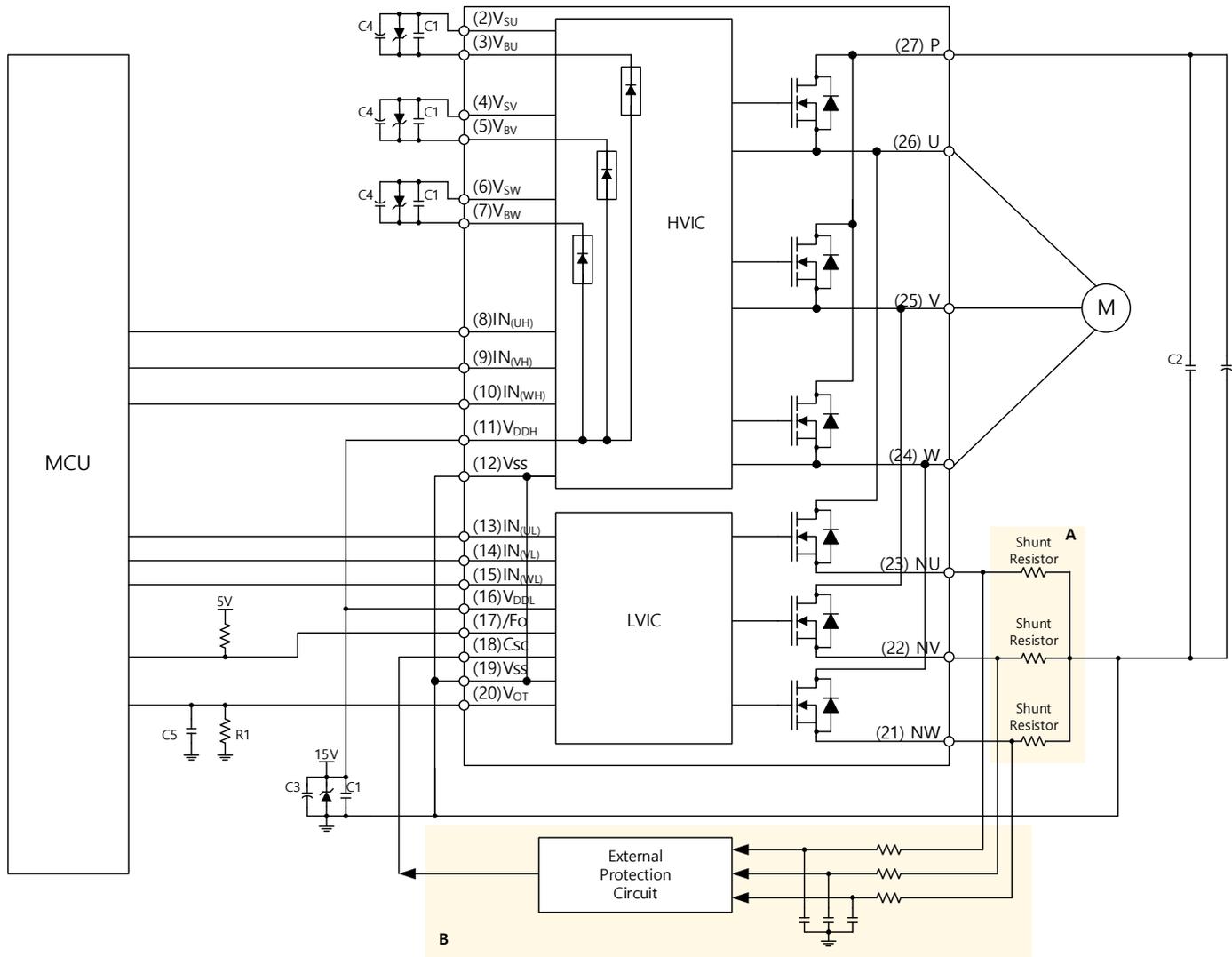
- 1: Normal operation: MOSFET ON and carrying current.
- 2: LVIC temperature exceeds OT trip level ( $OT_{trip}$ ).
- 3: All low-side MOSFETs OFF in spite of control input condition.
- 4: Fault output operation starts with a fixed pulse width (min. 20us).
- 5: LVIC temperature drop to OT reset level.
- 6: Normal operation: MOSFET ON and carrying current by triggering next signal from LOW to HIGH.

**Figure 11. Over-temperature Protection**



- 1: Normal operation: MOSFET ON and carrying current.
- 2: Short-circuit current detection (SC trigger).
- 3: All low-side MOSFETs gates are hard interrupted.
- 4: All low-side MOSFETs turn OFF.
- 5: Fault output operation starts with a fixed pulse width (min. 20us).
- 6: Input HIGH – MOSFET ON state, but during the active period of fault output, the MOSFET doesn't turn ON.
- 7: Fault output operation finishes, but MOSFET doesn't turn on until triggering the next signal from LOW to HIGH.
- 8: Normal operation: MOSFET ON and carrying current.

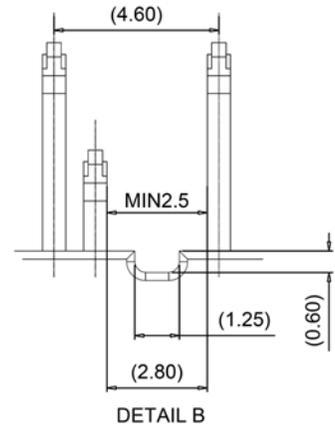
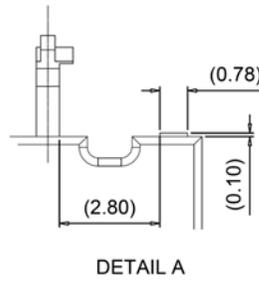
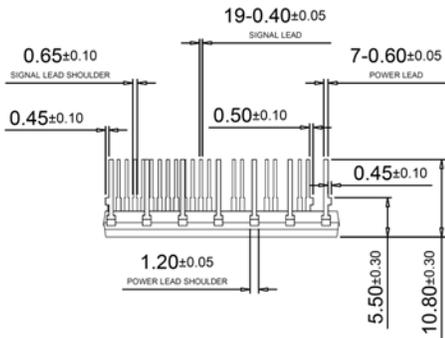
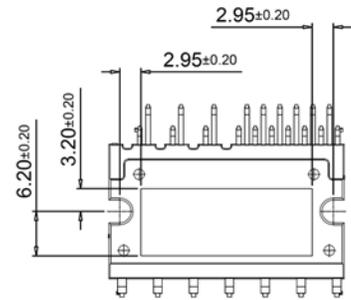
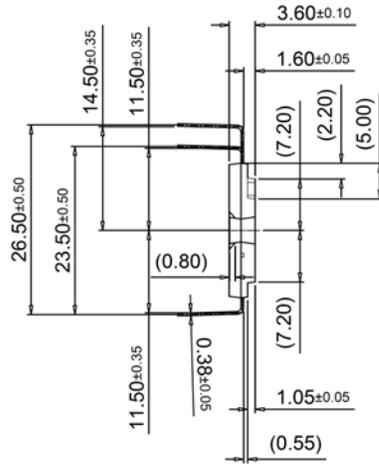
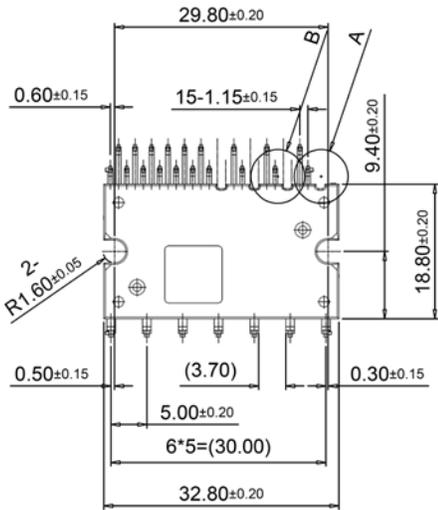
**Figure 12. Short-circuit Current Protection (Low-side Operation Only)**



**Figure 13. Typical Application Circuit**

1. To avoid malfunction, the wiring of each input should be as short as possible (less than 2~3 cm).
2. Fault output is an open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes  $I_{FO}$  up to 1 mA. Please refer to Figure 6.
3. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50~150 ns (recommended R = 100Ω, C = 1 nF). Please refer to Figure 6.
4. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor Rsh of surface mounted (SMD) type to reduce wiring inductance.
5. To insert the shunt resistor to measure each phase current at N<sub>U</sub>, N<sub>V</sub>, N<sub>W</sub> terminal, it makes to change the trip level I<sub>SC</sub> about the short-circuit current.
6. To prevent errors in the protection function, the wiring of point B should be as short as possible.
7. For stable protection function, use the sense resistor Rsh with resistance variation within 1% and low inductance value.
8. In the short-circuit protection circuit, select the RC time constant of protection circuit in the range 2.0~2.5 μs.
9. Each capacitor C1 should be mounted as close to the pins of the GPM product as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor C2 and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1~0.22 μF between the P & GND pins is recommended.
11. Relays are used in most systems of electrical equipment in industrial application. In these cases, there should be sufficient distance between the MCU and the relays.
12. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended Zener diode is 22V/1W, which has the lower Zener impedance characteristic than about 15 Ω).
13. C3 of around seven times larger than bootstrap capacitor C4 is recommended.
14. Please choose the electrolytic capacitor with good temperature characteristics in C4. Choose 0.1~0.2μF R-category ceramic capacitors with good temperature and frequency characteristics in C1.
15. For stable analog voltage output for LVIC temperature, please use ceramic capacitor for C5.

PACKAGE DIMENSIONS



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